

N-Channel Enhancement Mode Power MOSFET

Description

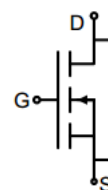
The GT52N10T uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

- V_{DS} 100V
- I_D (at $V_{GS} = 10V$) 80A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) $< 9m\Omega$
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) $< 15m\Omega$
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters
- Synchronous Rectification



Schematic Diagram



Marking and pin assignment



TO-220

Device	Package	Marking	Packaging
GT52N10T	TO-220	GT52N10	50pcs/Tube

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	100	V
Continuous Drain Current	I_D	80	A
Pulsed Drain Current (note1)	I_{DM}	320	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	227	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

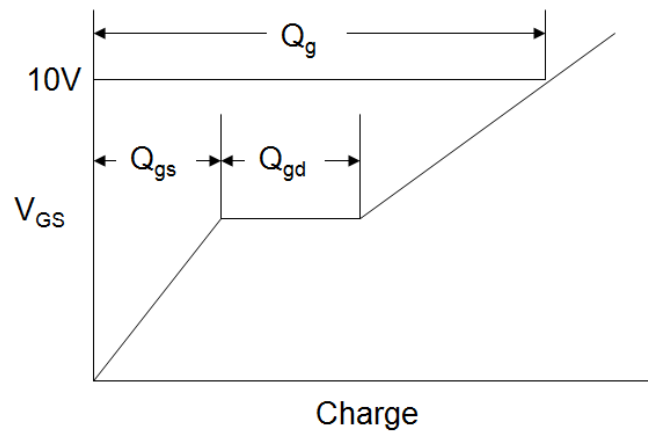
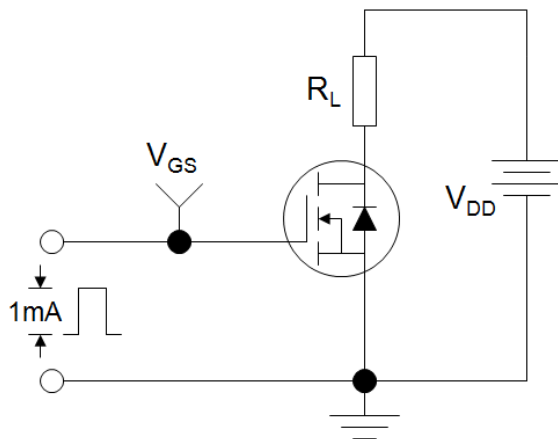
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	R_{thJC}	0.55	$^\circ\text{C/W}$

Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V	--	--	1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	1	1.6	2.5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D = 50A	--	6.3	9	mΩ
		V _{GS} = 4.5V, I _D = 50A	--	8	15	
Forward Transconductance	g _{FS}	V _{DS} =5V,I _D =50A	--	115	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 50V, f = 1.0MHz	--	2626	--	pF
Output Capacitance	C _{oss}		--	457	--	
Reverse Transfer Capacitance	C _{rss}		--	38	--	
Total Gate Charge	Q _g	V _{DD} = 50V, I _D = 50A, V _{GS} = 10V	--	44.5	--	nC
Gate-Source Charge	Q _{gs}		--	10.4	--	
Gate-Drain Charge	Q _{gd}		--	6.8	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = 50V, I _D = 50A, R _G = 3Ω	--	10.3	--	ns
Turn-on Rise Time	t _r		--	62	--	
Turn-off Delay Time	t _{d(off)}		--	30	--	
Turn-off Fall Time	t _f		--	98	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	80	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = 50A, V _{GS} = 0V	--	--	1.2	V

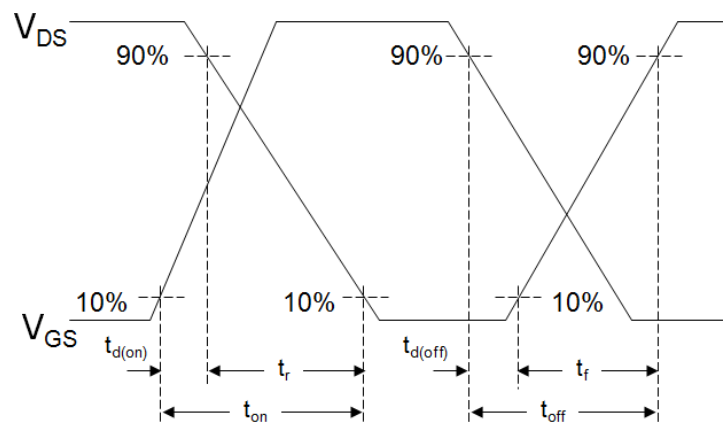
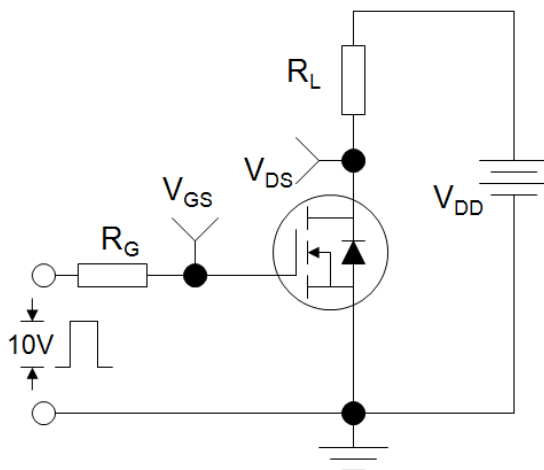
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $I_{AS} = 20A, V_{DD} = 40V, R_G = 25\Omega$, Starting $T_J = 25^{\circ}\text{C}$
3. Identical low side and high side switch with identical R_G

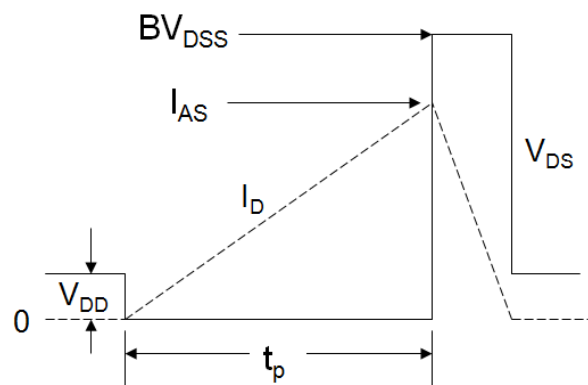
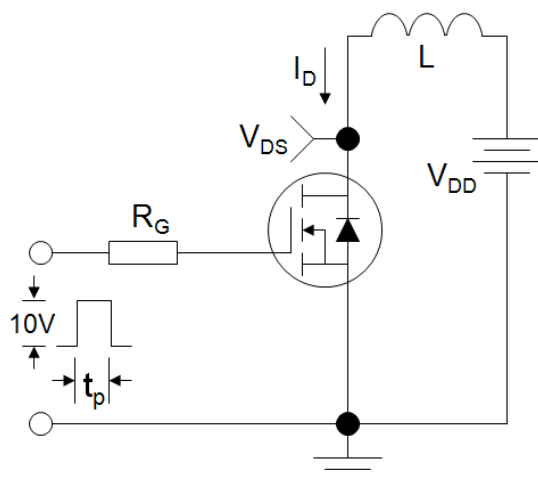
Gate Charge Test Circuit



EAS Test Circuit



Switch Time Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

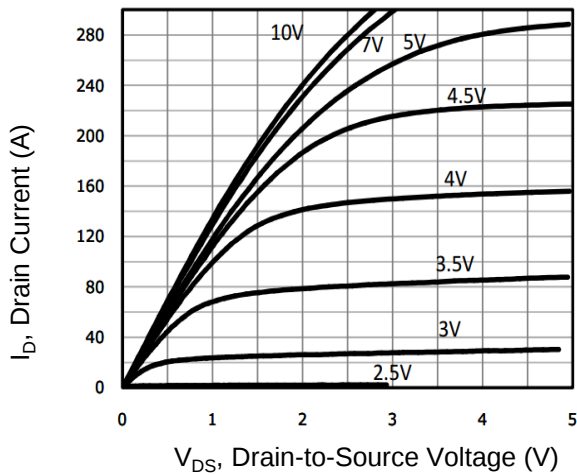


Figure 2. Transfer Characteristics

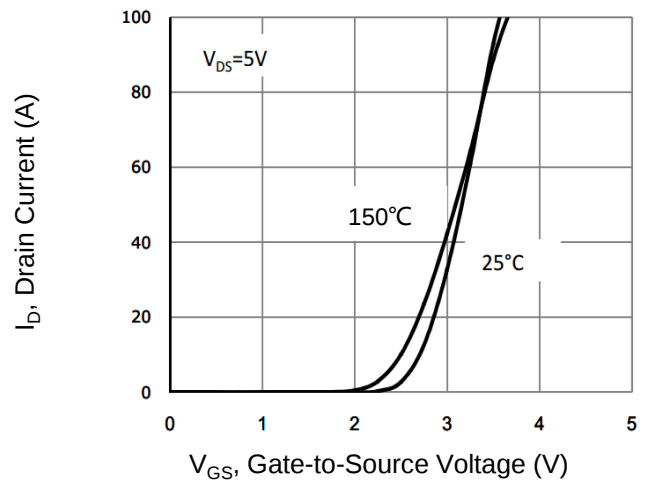


Figure 3. Gate Charge

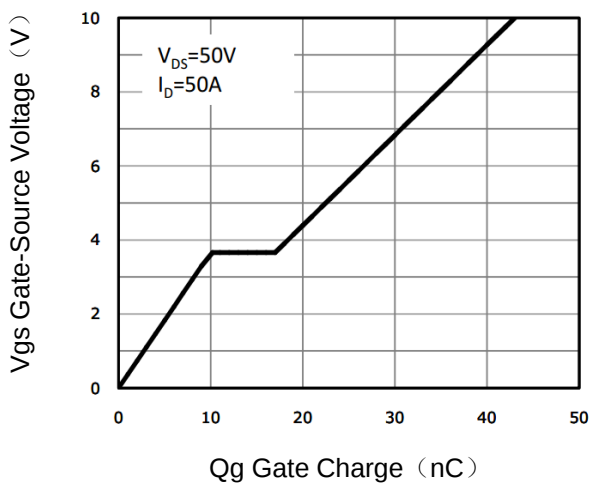


Figure 4. Drain Source On Resistance

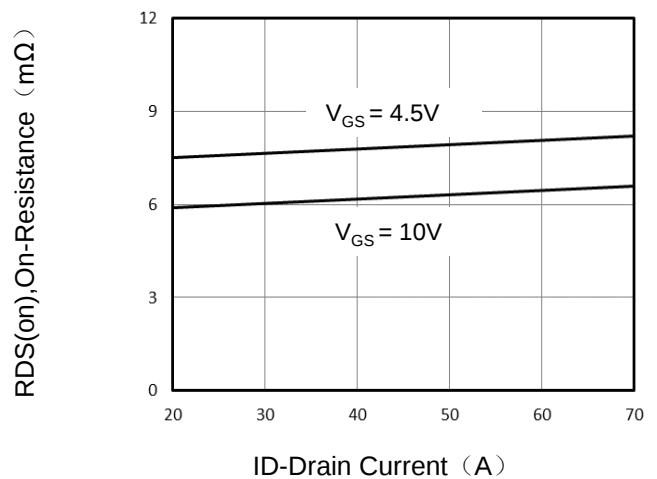


Figure 5. Capacitance vs Vds

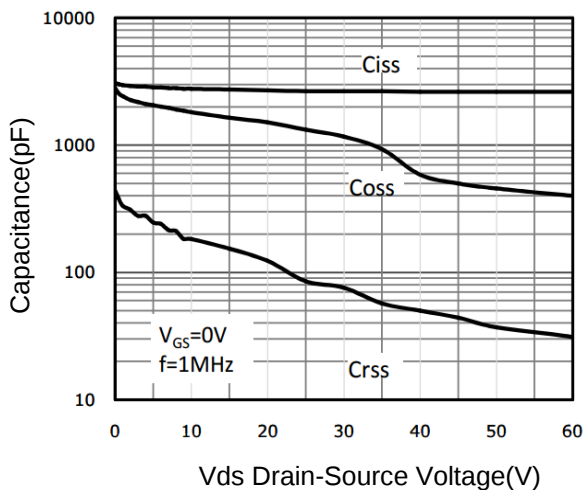
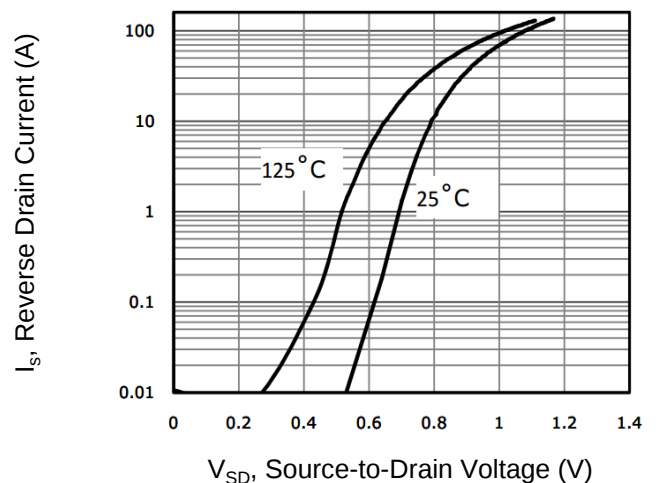


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

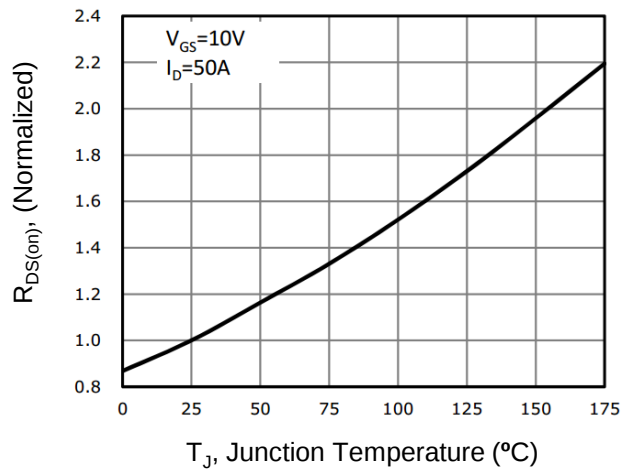


Figure 8. Safe Operation Area

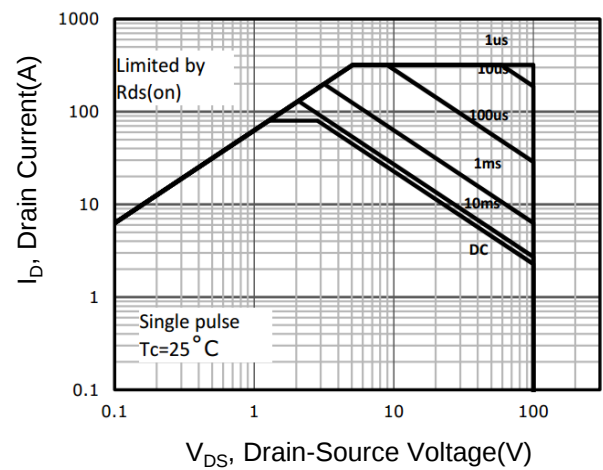
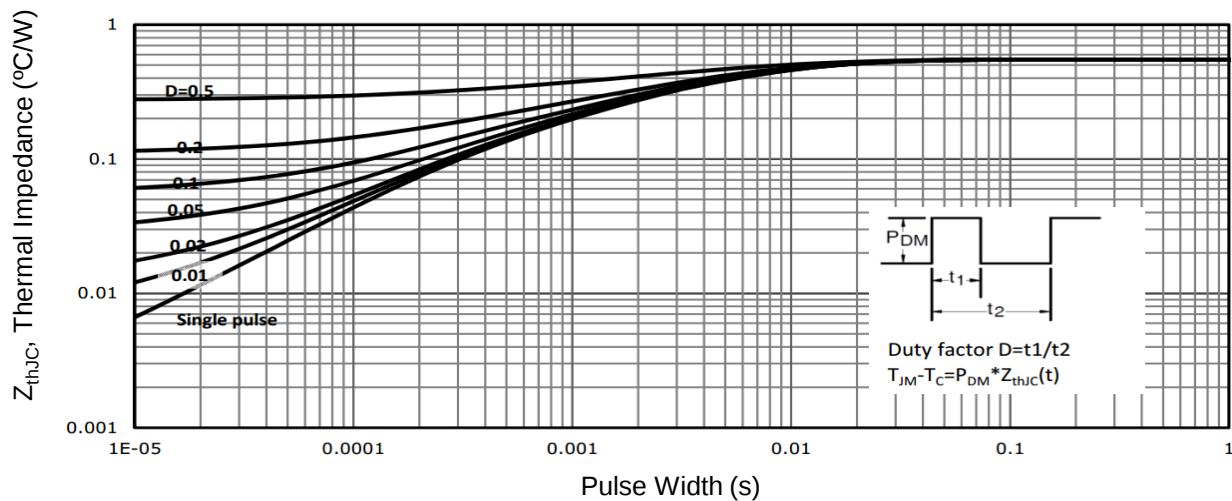
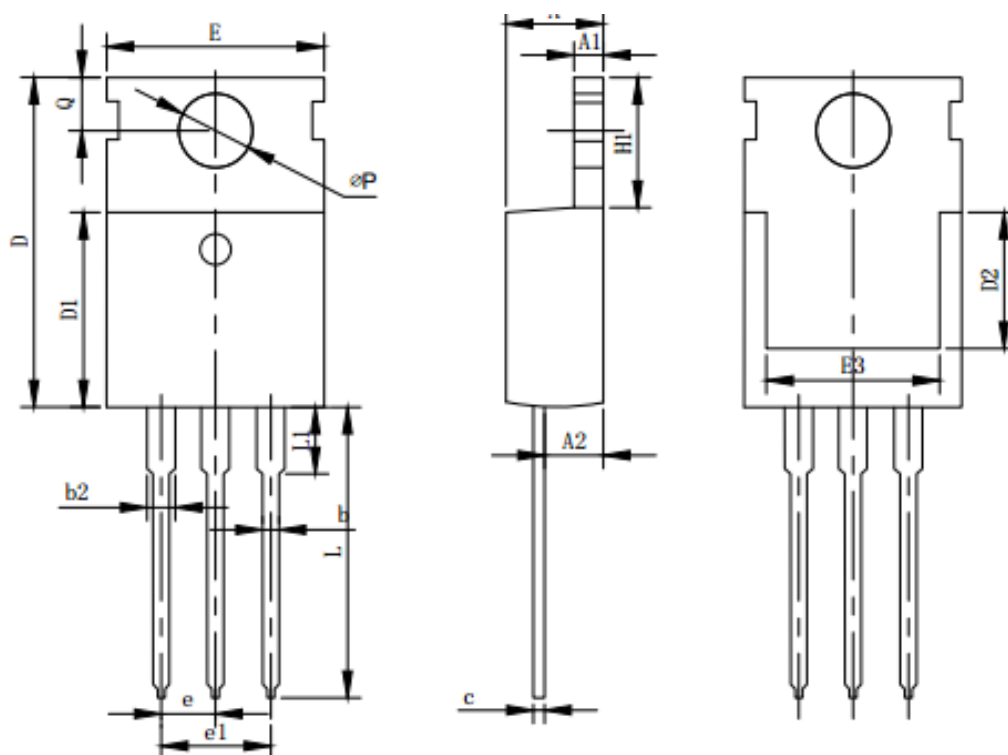


Figure 9. Normalized Maximum Transient Thermal Impedance



TO-220 Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	4.37	4.57	4.7
A1	1.25	1.3	1.4
A2	2.2	2.4	2.6
b	0.7	0.8	0.95
b2	1.7	1.27	1.47
c	0.45	0.5	0.6
D	15.1	15.6	16.1
D1	8.8	9.1	9.4
D2	5.5		
E	9.7	10	10.3
e	2.54BSC		
e1	5.08BSC		
H1	6.25	6.5	6.85
L	12.75	13.5	13.8
L1		3.1	3.4
øP	3.4	3.6	3.8
Q	2.6	2.8	3